PRESS RELEASE
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Tokyo Institute of Technology research: Reducing down to 1/3 of thermal resistance by WOW technology[1] for 3D DRAM application

(Tokyo, April, 2017) **Researchers at Tokyo institute of Technology presented a design guide for reducing 30% of thermal resistance for 3-dimensional (3D) stacked devices compared with the conventional ICs using solder bump joint structure.**

Researcher team led by Professor Takayuki Ohba at Tokyo Institute of Technology, ICE Cube Center, in collaboration with the WOW (Wafer-on-Wafer) Alliance[2], an Industry-academic collaborative research organization consisting of multiple semiconductor related companies aiming for practical applications of 3D IC technology, demonstrated the thermal resistance of the 3D stacked device can be reduced down to less than 1/3 relative to the conventional one bonded by bump[3] 3D IC in Through-Silicon-Via (TSV) wiring[4]. Since semiconductor circuits are highly heat-generating bodies during operation, when heat is hard to be released, the temperature of the semiconductor results in highly rise, which leads to be a malfunction. The development of heat dissipation technology has been a big challenge.

To address this challenge, Ohba and colleagues analyzed thermal properties in 3D IC using finite element method (FEM)[5] and thermal network calculation method. The study identified three main factors of thermal resistance; the interconnection layers, dielectric layers and organic layers in the conventional bump type device. Contrary to the bump type, the thermal performance of a bumpless 3D IC was almost 150 times better than that of a conventional IC at the same TSV density. The researchers demonstrated to reduce the total thermal resistance to 0.46 Kcm^2/W, whereas the conventional method is 1.54 Kcm^2/W. This suggests that the bumpless enables lower temperature rise and three to four times further DRAM stacking.

Based on their demonstration experiments, the scientists will work toward practical use of large-capacity memory technology for mobile terminals and servers.

The results of this research were reported at the International Conference of Electrics Packaging 2017 (ICEP2017) held in Tendo, Japan on April 19-21.

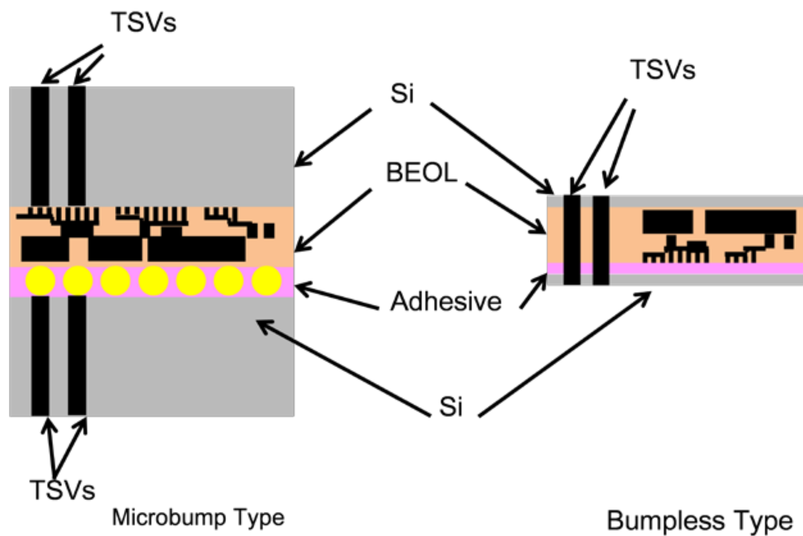

Figure. 1 Cross-sectional structure of micro bump and bumpless

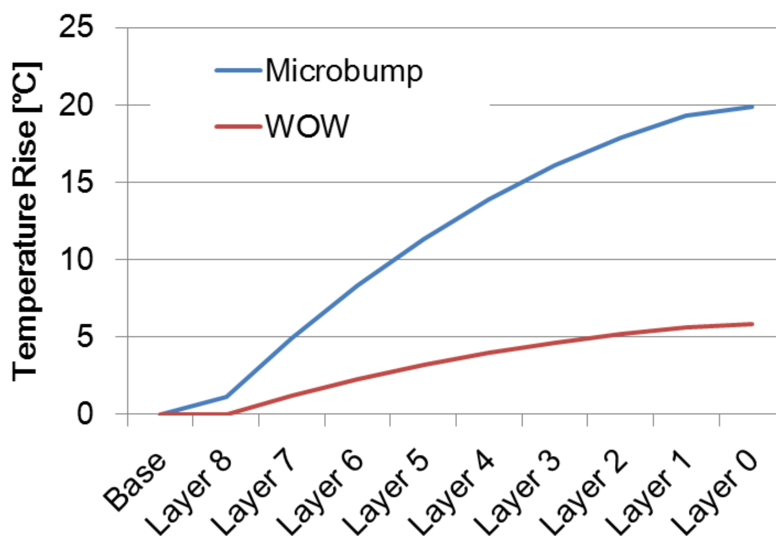

Figure 2. Comparison of temperature rise of micro bump and bumpless

Explanations of Technical Terms

1 **WOW 3D technology**: 3D integration technology for making large-scale integrated circuits by wafer stack (Wafer-on-Wafer). There is stack methods

including Chip-on-Chip (COC) and Chip-on-Wafer (COW) and productivity increased in the order of COC < COW < WOW.

2 **WOW Alliance**: A research group conducting at the Tokyo Institute of Technology and cooperated with semiconductor-related companies including design, process, device, materials, and research institutions. It succeeded in the world's first development of the bumpless TSV 3D technology, enabling wafer stack easily even thinned-down wafers.

3 **Bumps**: Joint metal material formed by electroplating method.

4 **TSV wiring** : Through-Silicon-Via wiring. A connection hole that penetrates the silicon wafer and connects the upper and lower chips with embedded wiring.

5 **FEM** : finite element method. A kind of numerical analysis method called finite element method.

Reference

H. Ryoson, K. Fujimoto, T. Ohba. A Design Guide of Thermal Resistance down to 30% for 3D Multi-stack Devices. *IEEE 2017 International Conference on Electronics Packaging (ICEP), pp. 822-825 (2017),* http://jiep.or.jp/icep/index.html

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